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| 10/804,945      | 03/19/2004  | Curtis R. Priem      | NVDA P000455        | 9182             |

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PATTERSON & SHERIDAN L.L.P.  
595 SHREWSBURY AVE, STE 100  
FIRST FLOOR  
SHREWSBURY, NJ 07702

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| EXAMINER |
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CLEARY, THOMAS J

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| ART UNIT | PAPER NUMBER |
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09/26/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/804,945

Applicant(s)

PRIEM, CURTIS R.

Examiner

Thomas J. Cleary

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 June 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15, 17, 18 and 20-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15, 17, 18 and 20-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-4, 9-10, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,826,081 to Zolnowsky ("Zolnowsky") and US Patent Number 5,812,844 to Jones et al. ("Jones").

3. In reference to Claim 1, Zolnowsky discloses a method for scheduling the service of a thread, said method comprising the steps of: masking interrupts from one or more hardware devices in order to ignore interrupts for other threads (See Column 6 Lines 34-42); acquiring information associated with a thread (see Column 6 Lines 45-52); unmasking interrupts from the one or more hardware devices in order to detect interrupts for the other threads (See Column 6 Lines 34-42); and rearranging an order in which the thread and the other threads will be serviced to schedule the thread for processing in accordance with said information (See Column 6 Lines 48-52).

Zolnowsky further discloses that there are a plurality of dispatch queues, and for each

single dispatch queue, a variety of different queuing mechanisms based on the information associated with the thread can be used for scheduling the threads associated with that queue depending on the real time application scheduling requirements (See Column 6 Lines 45-52). Zolnowsky further discloses that a real time operating system must be capable of scheduling a particular process within a fixed time limit (See Column 2 Lines 42-51). Zolnowsky does not explicitly disclose that the information regarding the thread is latency information and that the queuing mechanism (thread scheduler) used to sort each dispatch queue rearranges the order in which the threads will be serviced based on said latency information. Jones discloses the use of deadline scheduling in which the order in which threads are scheduled for execution is rearranged based on the latency of the thread (See Column 3 Lines 1-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Zolnowsky using a latency based queuing mechanism, resulting in the invention of Claim 1, because Zolnowsky discloses that any queuing mechanism can be used (See Column 6 Lines 45-52 of Zolnowsky). Because both references disclose mechanisms for queuing threads (thread schedulers), it would have been obvious to substitute one queuing mechanism for the other to achieve the predictable result of scheduling the threads for servicing and execution.

4. In reference to Claim 3, Zolnowsky and Jones disclose the limitations as applied to Claim 1 above. Jones further discloses computing the time at which the thread

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needs to be processed by summing the latency information with a current time (See Column 3 Lines 5-16).

5. In reference to Claim 4, Zolnowsky and Jones disclose the limitations as applied to Claim 1 above. Jones further discloses that said latency information represents a time duration that is necessary to service the thread (See Column 3 Lines 5-16).

6. Claim 9 recites limitations which are substantially equivalent to those of Claim 1 and is rejected under similar reasoning.

7. Claim 10 recites limitations which are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

8. In reference to Claim 20, Zolnowsky and Jones disclose the limitations as applied to Claim 1 above. Jones further discloses determining when the thread should be activated for processing using the latency information (See Column 3 Lines 6-12).

9. Claims 1-15, 17-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,085,215 to Ramakrishnan et al. ("Ramakrishnan") and Jones.

10. In reference to Claim 1, Ramakrishnan discloses a method for scheduling the service of a thread, said method comprising the steps of: masking interrupts from one or more hardware devices in order to ignore interrupts for other threads (See Column 4 Lines 44-48, Column 5 Lines 23-28, and Column 7 Lines 22-52); acquiring a latency information associated with a thread, wherein the latency information indicates a time at which the thread needs to be processed (See Column 10 Lines 48-64); and unmasking interrupts from the one or more hardware devices in order to detect interrupts for the other threads (See Column 4 Lines 44-48, Column 5 Lines 23-28, and Column 7 Lines 22-52). Ramakrishnan further discloses the use of deadline latency information when scheduling the threads (See Column 10 Lines 48-64), but does not disclose rearranging an order in which the thread and the other threads will be serviced in a single queue to schedule the thread for processing in accordance with said latency information. Jones discloses the use of deadline scheduling in which the order in which threads are scheduled for execution is rearranged based on the latency of the thread (See Column 3 Lines 1-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ramakrishnan with a latency based scheduling algorithm instead of a round robin scheduling algorithm, resulting in the invention of Claim 1, because Ramakrishnan discloses that the latency requirements of the thread are important when scheduling threads (See Column 10 Lines 48-64 of Ramakrishnan. Because both references disclose algorithms for queuing threads (thread schedulers), it would have been obvious to substitute one queuing algorithm for

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the other to achieve the predictable result of scheduling the threads for servicing and execution.

11. In reference to Claim 2, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses that said latency information is computed based on a buffer size (See Column 11 Lines 24-47).

12. In reference to Claim 3, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Jones further discloses computing the time at which the thread needs to be processed by summing the latency information with a current time (See Column 3 Lines 5-16).

13. In reference to Claim 4, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Jones further discloses that said latency information represents a time duration that is necessary to service the thread (See Column 3 Lines 5-16).

14. In reference to Claim 5, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses that said latency information represents a maximum time allowed before a first buffer will be emptied and a read operation will switch to process a second buffer (See Column 11 Lines 24-47).

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15. In reference to Claim 6, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses that said latency information represents a time duration that is necessary to setup the thread to perform interrupt processing for the thread (See Column 11 Lines 24-47).

16. In reference to Claim 7, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses that said latency information is dependant on a hardware constraint for one of the one or more hardware devices (See Column 11 Lines 24-47 and Column 12 Lines 43-55).

17. In reference to Claim 8, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses that said latency information is provided by a device driver (See Column 12 Lines 43-55).

18. Claim 9 recites limitations which are substantially equivalent to those of Claim 2 and is rejected under similar reasoning.

19. Claim 10 recites limitations which are substantially equivalent to those of Claim 3 and is rejected under similar reasoning.

20. Claim 11 recites limitations which are substantially equivalent to those of Claim 7 and is rejected under similar reasoning.



21. In reference to Claim 12, Ramakrishnan and Jones disclose the limitations as applied to Claim 11 above. Ramakrishnan further discloses that said hardware constraint is a size of a buffer (See Column 11 Lines 24-47).

22. In reference to Claim 13, Ramakrishnan and Jones disclose the limitations as applied to Claim 11 above. Ramakrishnan further discloses that said hardware constraint is a fullness of a buffer (See Column 11 Lines 24-47).

23. In reference to Claim 14, Ramakrishnan and Jones disclose the limitations as applied to Claim 11 above. Ramakrishnan further discloses that said hardware constraint is dynamically computed based on a buffer size (See Column 11 Lines 41-42).

24. Claim 15 recites limitations which are substantially equivalent to those of Claim 8 and is rejected under similar reasoning.

25. In reference to Claim 17, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses toggling an interrupt line (See Column 10 Lines 31-47).

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26. In reference to Claim 18, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses determining the thread should be activated; and activating the thread for processing (See Column 4 Lines 16-32).

27. In reference to Claim 20, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Jones further discloses determining when the thread should be activated for processing using the latency information (See Column 3 Lines 6-12).

1. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan and Jones as applied to Claim 1 above, and further in view of US Patent Application Publication Number 2002/0083143 to Cheng ("Cheng").

2. In reference to Claims 21 and 22, Ramakrishnan and Jones disclose the limitations as applied to Claim 1 above. Ramakrishnan further discloses creating threads for interrupt processing (See Column 10 Lines 34-37). Ramakrishnan and Jones do not disclose creating the thread for interrupt processing when one of the one or more hardware devices is initialized, wherein the thread is created for use during processing of a first interrupt that the one or more hardware devices is configured to generate; and freeing the thread when the one of the one or more hardware devices is shut down, as in Claim 21, and creating an additional thread, wherein a first interrupt identification number is associated with the thread and a second interrupt identification

number that is different than the first interrupt identification number is associated with the additional thread and the additional thread is created for use during processing of a second interrupt that the one of the one or more hardware devices is configured to generate; and freeing the additional thread when the one of the one or more hardware devices is shut down, as in Claim 22. Cheng discloses that it is well known to create a thread when a device is added to a system and to free a thread when a device is removed from a system (See Figure 6 and Paragraphs 67-73 and 24). The device of Cheng would inherently use different identification numbers for the thread, as the device would be inoperable the same identification number was used for multiple interrupt threads.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the thread creation of Cheng in the device of Ramakrishnan and Jones, resulting in the invention of Claims 21 and 22, because Ramakrishnan is silent as to how the threads are created and one of ordinary skill in the art would naturally look to methods of creating threads; and to allow both plug and play and non plug and play devices to be used in the same network system (See Abstract and Paragraphs 8 and 74).

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear as to what the absolute time refers to, as absolute time is the time with respect to a reference point, and it is unclear as to whether the reference point is the current time or another time.

### ***Claim Objections***

5. Claim 17 is objected to because of the following informalities: Claim 17 has not been amended in the amendment of 5 June 2007, but has a status identifier of "Currently Amended" instead of "Previously Presented". Appropriate correction is required.

### ***Response to Arguments***

6. Applicant's arguments with respect to Claims 1-15, 17-18, and 20-22 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant has argued that "the thread" is in reference to the claimed "a thread", and "the other threads" is in reference to the claimed "other threads" (See Page 6

Paragraph 2). As such, the Examiner will interpret “the thread” as referring only to “a thread”, and “the other threads” as referring only to “other threads”.

8. Applicant has argued that Zolnowsky does not disclose the rearrangement of the order of thread servicing in a single queue (See Page 7 Paragraph 3 – Page 8 Paragraph 1). In response, the Examiner notes that Zolnowsky discloses that each dispatch queue is separately ordered using a queuing mechanism when a thread for that dispatch queue is made runnable (See Column 6 Lines 43-52). Since each dispatch queue is a single queue, Zolnowsky discloses rearranging the order of thread servicing in a single queue.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC



**MARK H. RINEHART**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**



Thomas J. Cleary  
Patent Examiner  
Art Unit 2111